REMARKS

This is a full and timely response to the outstanding nonfinal Office Action mailed November 23, 2001. Reconsideration and allowance of the application and presently pending claims 1-10 and 14-32 are respectfully requested.

1. Present Status of Patent Application

Upon entry of the amendments in this response, claims 1-10 and 14-32 remain pending in the present application. More specifically, claims 11-13 have been cancelled, claims 26-32 have been added, and claim 18 has been directly amended.

2. Response to Rejection of Claim 18 Under 35 U.S.C. §112(1)

In the Office Action, claim 18 stands rejected under 35 U.S.C. §112, paragraph 1, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors...had possession of the claimed invention. Applicants have amended claim 18, which was originally meant to read as it now does, "forming a gate oxide above the semiconductor substrate; forming a first polysilicon layer over the gate oxide." Applicants respectfully assert that the gate oxide 16 and the first polysilicon layer 18 are shown, among other places, in FIGS. 1 and 4. Applicants would like to thank the Examiner for pointing out the Applicants' oversight in drafting the new claims, and indication of allowability of claims 18-25.

Furthermore, Applicants have corrected a grammatical error in claim 18, such that the claim now reads "an antireflective coating." This second change is not intended to have any effect on the patentability or scope of the claims. Applicants respectfully request reconsideration and withdrawal of the rejection with respect to claim 18-25, which are now in condition for allowance.

3. Response to Rejection of Claim 2 Under 35 U.S.C. §112

Applicants respectfully submit that in response to the previous Office Action (paper number 4), Applicants filed an amended claim 2 which does not include the phrase "anti-reflective coating," but rather includes the phrase "layer of silicon oxynitride." Applicants

respectfully assert that "...prior to the step of removing the remaining layer of silicon oxynitride," as the claim should now read, has antecedent basis in claim 1.

4. Response to Rejection of Claims 1-6, 10 and 14 Under 35 U.S.C. §103

In the Office Action, claims 1-6, 10 and 14 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Lee* (U.S. Patent 5,620,913) in view of *Fu* (U.S. Patent 6,245,682). It is well established at law that, for a proper rejection of a claim under 35 U.S.C. §103 as being obvious based upon a combination of references, the cited combination of references must disclose, teach, or suggest, either implicitly or explicitly, all features and/or steps of the claim at issue. See, *e.g.*, *In Re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981).

a. Claim 1

Assuming that the references are properly combinable and qualify as prior art, Applicants respectfully submit that claim 1 is allowable for at least the reason that the proposed combination of *Lee* in view of *Fu* does not disclose, teach, or suggest the step of "removing the remaining layer of silicon oxynitride by etching in hot phosphoric acid **before subjecting the layer of silicon oxynitride to any temperature greater than about 400°C**" (*emphasis added*) as recited in claim 1. That is, one embodiment, among others, of the present invention, as recited in claim 1, necessitates that the silicon oxynitride not be exposed to a temperature greater than about 400°C in order to achieve a reasonable etch rate.

Applicants submit that the combination of *Lee* in view of *Fu* does not disclose, teach, or suggest the concept of removing the silicon oxynitride before subjecting the silicon oxynitride to a temperature greater than about 400°C. The Office Action asserts that there is no recitation of such a limitation, but that it is inherently present because all of the steps are performed. Applicants respectfully direct the examiner to the *Fu* specification, lines 15-22. Here *Fu* specifically states "**said second protective oxide layer 16, is *thermally* grown...**" Applicants respectfully assert that the **thermal growth of an oxide layer is typically performed at temperatures well in excess of 400°C, and usually in excess of**

1000°C. However, as disclosed in the specification of the present Application, the etch rate of silicon oxynitride exposed as such is "about .2 nm per minute...at this etch rate, the amount of time required to remove silicon oxynitride layer 26 would cause serious etching of the exposed edge of the silicon nitride." Application specification, page 7, lines 17-23.

Applicants respectfully submit that it was not well known in the art that exposing silicon oxynitride to high temperatures hindered the etching process. Applicants respectfully submit that this may be why ***Fu* specifically recites the sidewall oxide deposition to protect the interpoly dielectric as "the key to this invention."** *Fu*, col. 5, lines 19-20. Therefore, Applicants respectfully assert that the combination of *Lee* in view of *Fu* does not and cannot disclose, teach or suggest the limitation as such, as recited in claim 1.

b. Claim 2-6

Because independent claim 1 is allowable over the prior art of record, dependent claims 2-6 (which depend either directly or indirectly from independent claim 1) are allowable as a matter of law for at least the reason that the dependent claims 2-6 contain all steps of independent claim 1. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

c. Claim 10

Assuming that the references are properly combinable and qualify as prior art, applicants respectfully submit that claim 10 is allowable for at least the reason that the proposed combination of *Lee* in view of *Fu* does not disclose, teach, or suggest the step of "etching the silicon oxynitride in a phosphoric acid etchant **without subjecting the layer of silicon oxynitride to any temperature greater than about 400°C between the steps of depositing and etching**" (*emphasis added*) as recited in claim 10. That is, one embodiment, among others, of the present invention, as recited in claim 10, necessitates that the silicon oxynitride not be exposed to a temperature greater than about 400°C in order to achieve a reasonable etch rate as outlined in the specification.

Applicants submit that the combination of *Lee* in view of *Fu* does not disclose, teach, or suggest the concept of removing the silicon oxynitride before subjecting the silicon

oxynitride to a temperature greater than about 400°C. The Office Action asserts that there is no recitation of such a limitation, but that it is inherently present because all of the steps are performed. Applicants respectfully direct the examiner to the *Fu* specification, lines 15-22. Here, specifically, it states "**said second protective oxide layer 16, is *thermally* grown...**" Applicants respectfully assert that the **thermal growth of an oxide layer is typically performed at temperatures well in excess of 400°C, and usually in excess of 1000°C**. However, as disclosed in the specification of this application, the etch rate of silicon oxynitride exposed as such is "about .2 nm per minute...at this etch rate, the amount of time required to remove silicon oxynitride layer 26 would cause serious etching of the exposed edge of the silicon nitride." Application specification, page 7, lines 17-23. The fact that a hot phosphoric acid etch is performed at a temperature between 100-150°C is of no consequence, since there has already been shown to be an exposure to temperatures in excess of 400°C.

Applicants respectfully submit that it was not well known in the art that exposing silicon oxynitride to high temperatures hindered the etching process. Applicants respectfully submit that this may be why ***Fu* specifically recites the sidewall oxide deposition to protect the interpoly dielectric as "the key to this invention."** *Fu*, col. 5, lines 19-20. Therefore, Applicants respectfully assert that the combination of *Lee* in view of *Fu* does not and cannot disclose, teach or suggest the limitation as such, as recited in claim 10.

d. Claim 14

Assuming that the references are properly combinable and qualify as prior art, Applicants respectfully submit that claim 14 is allowable for at least the reason that the proposed combination of *Lee* in view of *Fu* does not disclose, teach, or suggest the step of "etching the second layer in an etchant comprising hot phosphoric acid, the etching occurring **before the second layer is subjected to any temperature greater than about 400°C**" (*emphasis added*) as recited in claim 14. That is, one embodiment, among others, of the present invention, as recited in claim 14, necessitates that the silicon oxynitride not be

exposed to a temperature greater than about 400°C in order to achieve a reasonable etch rate as outlined in the specification.

Applicants submit that the combination of *Lee* in view of *Fu* does not disclose, teach, or suggest the concept of removing the silicon oxynitride before subjecting the silicon oxynitride to a temperature of greater than about 400°C. The Office Action asserts that there is no recitation of such a limitation, but that it is inherently present because all of the steps are performed. Applicants respectfully direct the examiner to the *Fu* specification, lines 15-22. Here, specifically, it states "**said second protective oxide layer 16, is *thermally* grown...**" Applicants respectfully assert that the **thermal growth of an oxide layer is typically performed at temperatures well in excess of 400°C, and usually in excess of 1000°C**. However, as disclosed in the specification of this application, the etch rate of silicon oxynitride exposed as such is "about .2 nm per minute...at this etch rate, the amount of time required to remove silicon oxynitride layer 26 would cause serious etching of the exposed edge of the silicon nitride." Application specification, page 7, lines 17-23. The fact that a hot phosphoric acid etch is performed at a temperature between 100-150°C is of no consequence, since there has already been shown to be an exposure to temperatures in excess of 400°C.

Applicants respectfully submit that it was not well known in the art that exposing silicon oxynitride to high temperatures hindered the etching process. Applicants respectfully submit that this may be why ***Fu* specifically recites the sidewall oxide deposition to protect the interpoly dielectric as "the key to this invention."** *Fu*, col. 5, lines 19-20. Therefore, Applicants respectfully assert that the combination of *Lee* in view of *Fu* does not and cannot disclose, teach or suggest the limitation as such, as recited in claim 14.

5. Response to Rejection of Claims 7-9 and 15-17 Under 35 U.S.C. §103

In the Office Action, claims 7-9 and 15-17 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Lee* (U.S. Patent 5,620,913) in view of *Fu* (U.S. Patent 6,245,682), as applied to claims 1 and 14, and further in view of *Cheung* (U.S. Patent 5,968,324). It is well established at law that, for a proper rejection of a claim under 35

U.S.C. §103 as being obvious based upon a combination of references, the cited combination of references must disclose, teach, or suggest, either implicitly or explicitly, all features and/or steps of the claim at issue. See, *e.g.*, *In Re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981).

a. Claim 7-9 and 15-17

Because independent claims 1 and 14 are allowable over the prior art of record, dependent claims 7-19 and 15-17 (which depend either directly or indirectly from independent claims 1 and 14, respectively) are allowable as a matter of law for at least the reason that the dependent claims 7-9 and 15-17 contain all steps of independent claims 1 and 14, respectively. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

6. Response to Rejection of Claims 10 and 14 Under 35 U.S.C. §103

In the Office Action, claims 10 and 14 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Adkisson* (U.S. Patent 6,030,541). It is well established at law that, for a proper rejection of a claim under 35 U.S.C. §103 as being obvious based upon a combination of references, the cited combination of references must disclose, teach, or suggest, either implicitly or explicitly, all features and/or steps of the claim at issue. See, *e.g.*, *In Re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981).

a. Claim 10

Applicants respectfully submit that claim 10 is allowable for at least the reason that *Adkisson* does not disclose, teach, or suggest the step of "etching the silicon oxynitride in a phosphoric acid etchant **without subjecting the layer of silicon oxynitride to any temperature greater than about 400°C between the steps of depositing and etching**" (*emphasis added*) as recited in claim 10, and this would not have been obvious to one of ordinary skill in the art. That is, one embodiment, among others, of the present invention, as recited in claim 10, necessitates that the silicon oxynitride not be exposed to a

temperature greater than about 400°C in order to achieve a reasonable etch rate as outlined in the specification.

Applicants respectfully assert that *Adkisson* does not disclose, teach, or suggest the concept of not exposing the silicon oxynitride to a temperature of greater than 400°C. The Office Action states that there is no recitation of such a limitation, but that it must be inherently present because all of the other steps are performed. Applicants respectfully submit that the Office Action means to say that the temperature limitation is well known in the art, since inherency of the limitation would have raised a novelty rejection rather than an obvious rejection.

The mere fact that a reference does not recite the performance of the negative limitation does not mean that it renders that negative limitation obvious. Applicants respectfully submit that the silicon oxynitride may be etched even after exposure to a temperature above 400°C. However, the etch rate of an exposed silicon oxynitride as such is "about .2 nm per minute...at this etch rate, the amount of time required to remove silicon oxynitride layer 26 would cause serious etching of the exposed edge of the silicon nitride." Application specification, page 7, lines 17-23.

Adkisson does not specifically point out a temperature higher than 400°C, however, *Adkisson* contains the same recitation of developing an oxide on top of the silicon oxynitride layer "in order to prevent poisoning or acidification from the photoresist." *Adkisson*, column 4, lines 33-40. Applicants respectfully assert that although this step cites no temperature, it **would lead one skilled in the art to believe that a thermal oxidation would be desirable or *at least* that subsequent processing steps which exposed the silicon oxynitride layer to temperatures above 400°C were acceptable**, thereby teaching away from the claims of the present invention. Applicants respectfully assert that this teaching is proof that it was not well known that exposing the silicon oxynitride to high temperatures would result in an extremely slow etch rate. Therefore, Applicants respectfully assert that *Adkisson* does not disclose, teach, or suggest the limitation as such, as recited in claim 10.

b. Claim 14

Applicants respectfully submit that claim 14 is allowable for at least the reason that *Adkisson* does not disclose, teach, or suggest the step of "etching the second layer in an etchant comprising hot phosphoric acid, the etching occurring **before the second layer is subjected to any temperature greater than about 400°C**" (*emphasis added*) as recited in claim 14, and this step would not have been obvious to one of ordinary skill in the art. That is, one embodiment, among others, of the present invention, as recited in claim 14, necessitates that the silicon oxynitride not be exposed to a temperature greater than about 400°C in order to achieve a reasonable etch rate as outlined in the specification.

Applicants respectfully submit that *Adkisson* does not disclose, teach, or suggest the concept of removing the silicon oxynitride prior to subjecting the silicon oxynitride to a temperature of greater than 400°C. The Office Action states that there is no recitation of such a limitation, but that it must be inherently present because all of the other steps are performed. Applicants respectfully submit that the Office Action means to say that the temperature limitation is well known in the art or obvious, since inherency of the limitation would have raised a novelty rejection rather than an obviousness rejection.

The mere fact that a reference does not recite the performance of the negative limitation does not mean that it renders that negative limitation obvious. Applicants respectfully submit that the silicon oxynitride may be etched even after exposure to a temperature above 400°C. However, the etch rate of an exposed silicon oxynitride as such is "about .2 nm per minute...at this etch rate, the amount of time required to remove silicon oxynitride layer 26 would cause serious etching of the exposed edge of the silicon nitride." Application specification, page 7, lines 17-23. Thus, the fact that the end product may *or may not* be the same is not the correct focus of this inquiry. Thus, it may be possible to produce and end product, even if the teachings of the present Applicant are ignored.

Adkisson does not specifically point out a temperature higher than 400°C, however, *Adkisson* contains the same recitation of developing an oxide on top of the silicon oxynitride layer "in order to prevent poisoning or acidification from the photoresist." *Adkisson*, column 4, lines 33-40. Applicants respectfully assert that although this step cites no temperature, it **would lead one skilled in the art to believe that a thermal oxidation**

would be desirable or *at least* that subsequent processing steps which exposed the silicon oxynitride layer to temperatures above 400°C were acceptable, teaching away from the claims of the present invention. Applicants respectfully assert that this teaching is proof that it was not well known that exposing the silicon oxynitride to high temperatures would result in an extremely slow etch rate. Therefore, Applicants respectfully assert that *Adkisson* does not disclose, teach or suggest the limitation as such, as recited in claim 10.

Further, Applicants respectfully submit that claim 14 is allowable for at least the reason that *Adkisson* does not disclose, teach, or suggest the step of "etching the second layer in an etchant comprising **hot** phosphoric acid..." (*emphasis added*) as recited in claim 14. That is, one embodiment of the present invention, as recited in claim 14, uses ***hot*** phosphoric acid to etch the silicon oxynitride layer.

Applicants believe that *Adkisson* does not disclose, teach, or suggest the concept of using "**HOT**" phosphoric acid to etch the silcon oxynitride layer. **It appears from the specification of *Adkisson* that the etchant is "*aqueous* phosphoric acid.**" *Adkisson*, column 5, lines 29-35. Applicants respectfully assert that *aqueous* phosphoric acid and **hot** phosphoric acid are not equivalent, since their respective etch rates are not equivalent, and thus the Office Action has not born its duty to prove a prima facie case of obviousness. Thus, Applicants respectfully assert that *Adkisson* does not teach, suggest or disclose the limitation as recited in claim 14.

7. <u>Response to Rejection of Claims 15-17 Under 35 U.S.C. §103</u>

In the Office Action, claims 15-17 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Adkisson* (U.S. Patent 6,030,541), as applied to claim 14, and in view of *Cheung* (U.S. Patent 5,968,324). It is well established at law that, for a proper rejection of a claim under 35 U.S.C. §103 as being obvious based upon a combination of references, the cited combination of references must disclose, teach, or suggest, either implicitly or explicitly, all features and/or steps of the claim at issue. See, *e.g.*, *In Re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981).

a. Claims 15-17

Because independent claim 14 is allowable over the prior art of record, dependent claims 15-17 (which depend either directly or indirectly from independent claim 14) are allowable as a matter of law for at least the reason that the dependent claims 15-17 contain all steps of independent claim 14. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

8. Allowability of Added Claims

a. Claim 26

Claim 26 contains the limitation noted as allowable in the present Office Action, *i.e.* "removing the antireflective coating without applying an oxide between the formation of the anti-reflective coating and the removal of the anti-reflective coating." Applicants respectfully assert that none of the presently cited references shows this claimed limitation. Therefore, Applicants respectfully assert that newly added claim 26 is in condition for allowance.

b. Claims 27-32

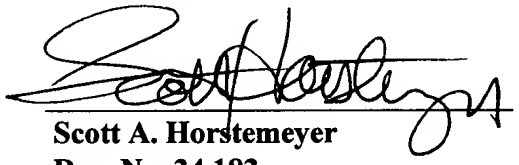
Because independent claim 26 is allowable over the prior art of record, dependent claims 27-32 (which depend either directly or indirectly from independent claim 26) are allowable as a matter of law for at least the reason that the dependent claims 27-32 contain all steps of independent claim 26. See, *e.g.*, *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicants respectfully submit that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1-10 and 14-32 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

THOMAS, KAYDEN,
HORSTEMEYER & RISLEY, L.L.P.

By: 

Scott A. Horstemeyer
Reg. No. 34,183

100 Galleria Parkway N.W.
Suite 1750
Atlanta, Georgia 30339
(770) 933-9500

ANNOTATED VERSION OF MODIFIED CLAIMS SHOWING CHANGES MADE

Amend the following claims by adding the language that is underlined ("___") and by deleting the language that is enclosed within brackets ("[ ]"):

18. (NEW) A process comprising:

providing a semiconductor substrate;

forming a gate oxide above the semiconductor substrate;

forming a first polycrystalline silicon layer over the gate oxide;

forming an interpoly dielectric;

forming a second polycrystalline silicon layer over the interpoly dielectric;

forming an anti-reflective coating above the second polycrystalline silicon layer;

patterning the device to form a stack; and

removing the antireflective coating without applying an oxide between the formation of the anti-reflective coating and the removal of the anti-reflective coating.